#18/Appeal Brief

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Chow, Chung-kai; De Angel, Edwin; Lee, Wai Laing; Page, Joel; Wang, Lei; Zheng, Hong
Assignee:	Cirrus Logic, Inc.
Title:	Power On Reset Techniques For An Integrated Circuit Chip
Serial No.:	~~09/153,364~~ 09/153,864 Filing Date: September 16, 1998
Examiner:	Jeffrey S. Zweizig Group Art Unit: 2816
Docket No.:	M-11434 US

3/20/01

San Jose, California
February 28, 2001

BOX AF
COMMISSIONER FOR PATENTS
Washington, D. C. 20231

APPEAL BRIEF

Dear Sir:

This Appeal Brief is submitted in triplicate in support of the appeal of the above-identified patent application. A Notice of Appeal was filed in this case on December 28, 2000. Please charge deposit account No. 19-2386 for the fee of $310.00 associated with this appeal brief. No extension of time is believed to be necessary. However, in the event that an extension of time is required, that extension of time is hereby requested. Please charge any fee associated with an extension of time to Deposit Account No. 19-2386. Please charge this deposit account for any additional sums which may be required to be paid as part of this appeal.

REAL PARTY IN INTEREST

The real party in interest to the subject application in this appeal is Cirrus Logic, Inc., the assignee of record.

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RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, the Appellants' legal representative, or assignee, which directly effect or would be directly effected by or have a bearing on the Board's decision in the pending appeal.

STATUS OF CLAIMS

When originally filed, the subject application included 17 claims. In the first Office Action, the Examiner set forth a restriction requirement between claims 1-13 and claims 14-17. In response to that Action, Appellants filed a petition to reconsider the restriction requirement, and provisionally elected claims 1-13 for continued prosecution. In the second Office Action, the Examiner rejected claims 1-13 under § 112, first and second paragraphs, and rejected claims 1, 6, 7, and 12 under § 102(b) as being anticipated by Shaik. In response to that action, Appellants filed a response and made amendments to claims 1 and 7 which were solely of a grammatical nature. The Examiner, thereafter, issued a third (and final) Office Action maintaining the rejection of claims 1-13 under § 112, first and second paragraphs, and the rejection of claims 1, 6, 7, and 12 under § 102(b).

Claims 1-13 remain pending, and stand finally rejected as noted by the Examiner in the final Office Action dated September 29, 2000. The rejection of all of these claims (which are set forth in the Appendix) is being appealed.

STATUS OF AMENDMENTS

No amendment has been filed subsequent to the final rejection that led to this appeal.

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SUMMARY OF THE INVENTION

The present invention operates in a data processing system having multiple clock circuits which require synchronization. In an illustrative implementation, the present invention assists with the acquisition of seismic data from a large number of seismic sensors. Synchronization of data gathered from a seismic explosion is often difficult because the timing of the explosion with respect to the triggering signal is often unpredictable, particularly with such explosive agents as dynamite.

In accordance with an important aspect of the present invention, a mechanism is provided which inhibits all clock activity used for digital logic operations associated with the seismic data acquisition until voltage stability within the digital circuits is achieved. In particular, when the power supply voltage is applied to the integrated circuit and exceeds a preset threshold, a phase-locked loop begins operation, but the clock circuits are initially inhibited. Once the applied voltage approaches the full level of the power supply, i.e., once voltage stability is achieved, the hold on the operation of the clock circuits is released. Inhibition of the clock circuits may be achieved by setting the duty cycle of a switched converter to unity until voltage stability has been achieved. The duty cycle of the switched converter is reduced from unity after its output reaches substantially the power supply voltage. The clock circuits may be released in stages.

ISSUES ON APPEAL

The ultimate questions to be resolved on this appeal are (i) whether claims 1-13 are sufficiently enabled by the specification, (ii) whether claims 1-13 are indefinite when read in light of the specification, and (iii) whether claims 1, 6, 7, and 12 are anticipated by Shaik. The § 112 rejections are essentially controlled by one paramount issue, namely, whether one

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skilled in the art, upon reference to Appellants' specification, would understand the invention and be able to practice it without undue experimentation. The § 102(b) rejection is controlled by the issue of whether Shaik discloses a circuit which starts a phase-locked loop when voltage is applied and exceeds a preset threshold, while inhibiting operation of clock circuits, and thereafter releasing the inhibited clocks once a voltage stability has been achieved. With regard to the § 102(b) rejection, that issue would be dispositive of all of the pending claims since each independent claim includes the above-noted recitation regarding the starting of a phase-locked loop upon the applied voltage exceeding a preset threshold, while inhibiting at least one clock circuit, and thereafter releasing the clock circuits upon reaching voltage stability.

GROUPING OF CLAIMS

The claims all stand or fall together with respect to each ground of rejection. Regarding the § 112, first paragraph rejections, each of the independent claims includes similar recitations regarding application of the supply voltage, the starting of a phase-locked loop, inhibition of clock operations, and finally, release of the inhibited clocks upon reaching voltage stability. Regarding the § 112, second paragraph rejections, each of the independent claims also contain reference to the phase-locked loop and the inhibited clocks. With regard to the § 102(b) rejections, independent claims 1 and 12 both contain the explicit recitations regarding the starting of a phase-locked loop upon the applied voltage exceeding a preset threshold, and the releasing of the hold of the operations of the clock circuits.

ARGUMENT

This Appeal is being filed in response to the Office Action final rejection dated September 29, 2000. In that Action, the Examiner rejected all pending claims under § 112,

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first and second paragraphs. Claims 1, 6, 7, and 12 were further rejected as being anticipated by Shaik under § 102(b). With respect to all of the rejections, Appellants' would first incorporate by reference the arguments and authorities set forth in the previously filed responses. More particularly, Appellants' would reiterate that one skilled in the art, upon reference to Appellants' specification, would not only understand what is being claimed by Appellants, but further would be able to reproduce the invention without undue experimentation. Appellants would further reiterate that Shaik generally fails to teach the gist of the present invention, that is, the inhibition of clock circuits until voltage stability has been achieved.

A. The § 112, First Paragraph Rejections

Appellants initially note that it is the examiner's burden to prove a lack of enablement. The Examiner has not carried this burden but, rather, has merely made conclusory statements without undertaking the analysis outlined in MPEP § 2164.01(a).

The original disclosure of the invention in this case is more than sufficient to enable a person skilled in the art of electronic circuit design to make and use the invention without undue experimentation. The Examiner incorrectly asserts that the recitations in the claims regarding the power on reset (POR) circuit of the present invention do not have support in the specification. This assertion is clearly incorrect as the POR circuit is discussed in detail several places in the specification. The POR circuit is illustrated in Figure 7 as reference numeral 795. Page 31, lines 32-35 of Appellants' specification notes that this POR circuit uses the novel protocol of the present invention to advantageously ensure the correct start up of the integrated circuit chip. Page 32, lines 1-21, explain in detail the operation of POR circuit 795. It is there explained that the supply voltage (V_{DD}, e.g., 5 volts) is applied to POR circuit 795. Once the value of the applied V_{DD} rises to a point which exceeds three times the

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threshold voltage of the devices in question, POR circuit 795 is activated. While no detailed schematic is provided which shows the exact manner in which the power on reset circuit is activated in response to the application of the power supply voltage, such details are well within the knowledge of one skilled in the art. Certainly, the Examiner is not arguing that it would require undue experimentation to construct a power on reset circuit which is activated only when a preset threshold voltage is applied. As noted in the MPEP, the fact that experimentation may be required does not necessarily make it undue, even if it requires complex experimentation. Indeed, it is clear that no experimentation is required for this aspect of the present invention. Power on reset circuits are generally known, as are threshold voltage detection circuits.

The Examiner also complains that the power on reset circuit of the figures does not show the "first circuit" or "starting circuit" of the claims. This complaint is appropriately addressed by an objection to the drawings, and not by a § 112, first paragraph rejection. The Examiner also states that the switch converter or regulator is not shown in the drawings, but this feature is illustrated in Figure 7 as reference numeral 770 (and denoted in that Figure as "regulator/SC converter"). The regulator/switch converter is also discussed in detail with reference to Appellants' Figures 23 and 24. Figure 23 is a schematic diagram of one embodiment of the switched power converter used by the present invention, while Figure 24 is a schematic diagram of an exemplary break-before-make-circuit used with the switched power converter of Figure 23. These figures are discussed in detail at pages 30-31.

The Examiner also complains that the phase-locked loop (PLL) and the clocks are not shown in Figure 7. Again, this complaint is more properly addressed by an objection to the drawings; however, it is not necessary that these elements be shown in detail. As set forth in 37 C.F.R. § 1.83(a), "conventional features disclosed in the description and claims, where

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their detailed illustration is not essential for a proper understanding of the invention, should be illustrated in the drawing in the form of a graphical drawings symbol or a labeled representation." It is indisputable that PLLs and clock circuits are generally well known in the art, and so their detailed illustration is not required under Rule 83. Moreover, the specification notes that the PLL is contained within the clock recovery and reset logic (illustrated as reference numeral 725 in Figure 7); *see* page 33, lines 15-18.

The § 112, first paragraph rejection also states that the POR circuit is shown as being isolated from the rest of the circuitry in Figure 7, and consequently, it is not understood how the POR circuit would interact with the PLL or the plurality of clocks. First of all, it is not necessary to explicitly illustrate the interconnection of these various components; the test of enablement is not whether the drawings show such an interconnection, but rather whether the construction of such an interconnection would involve undue experimentation. Appellants would respectfully submit that, even in the absence of any explanation in the specification, the details of such an interconnection would become apparent to one skilled in the art. Moreover, Appellants' specification does indeed explain how these various components communicate or interact. Specifically, several different buses are shown in Figure 7 which allow these communications. In particular, page 31, lines 10-14 note that the "TMI bus" shown in Figure 7 may be used to provide communications with the regulator/SC converter, and this bus is clearly illustrated in Figure 7 as also providing an interconnection with the clock recovery and reset logic 725. While these interconnections could have been more explicitly shown, there is no question that the interconnection of the POR circuit, the switched converter, and the clock control logic is a matter that would be simple to implement for one skilled in the art.

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Finally, the Examiner has stated that the specification discloses no means to perform the methods recited in claims 8-13, as well as the circuit or component that is responsible for

performing the action recited in part "c" of claim 1. This portion of the Examiner's rejection completely disregards the detailed explanation of these functions, particularly as explained with reference to Figure 25. Figure 25 is a timing diagram that illustrates the operation of the power on reset circuit as it effects the PLL and clock circuits. This figure and the associated text explicitly describe all of the steps in the claimed method.

B. The § 112, Second Paragraph Rejections

Many of the foregoing arguments also apply to the § 112, second paragraph rejections. Appellants would initially note that it is axiomatic that claim language should be read in light of the specification, as it would be interpreted by one of ordinary skill in the art. In rejecting a claim under the second paragraph of § 112, it is incumbent on the examiner to establish that one of ordinary skill in the pertinent art, when reading the claims in light of the supporting specification, would not have been able to ascertain with a reasonable degree of precision and particularity the particular area set out and circumscribed by the claims. Contrary to this requirement, the Examiner has disregarded the details in the specification which support Appellants' claim language.

The Office Action states that the examiner does not understand "toward what" the various claimed elements are directed. These statements are generally nonsensical, as the PLL and clocks are not "directed" toward any particular element but, rather, stand by themselves with the interconnected functionality as explicitly recited in the claims. For example, in claim 1, the first circuit is recited as being used to apply a voltage to the power on reset circuit. This first circuit is thus merely a power supply, and one skilled in the art would have no difficulty in understanding it as such. Claim 1 further recites that the second circuit is used to start the PLL when the applied voltage exceeds a preset threshold. Again, Appellants' cannot image that the Examiner is actually arguing that one skilled in the art would not

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understand how a circuit could enable a phase-locked loop upon an applied voltage threshold being met. The plain language of claim 1 is easily understandable by one skilled in the art, without even necessitating any reliance on the supporting specification -- one skilled in the art would have no trouble understanding what a PLL is, or that it is activated only when the applied voltage exceeds the threshold. Likewise, the language "inhibiting operation of at least a plurality of clocks" is equally clear. The meaning of the term "inhibit" is the same as the common and ordinary meaning of that term, namely, operation of the clock circuits is simply precluded; this aspect of the invention is also not difficult to understand. Finally, the "release" of the clocks upon voltage stability being achieved is also straightforward. There is no difficulty in understanding voltage stability. The Examiner questions which components set the threshold, and release the inhibited clocks, but it is not necessary to describe that level of detail in Appellants' broadest claims. Indeed, those details are set forth in dependent claims, which specify that the duty cycle of the switched converter is maintained at unity until the output of the converter substantially reaches the power supply voltage.

The Examiner also questions the nature of the switched converter, but that component is described and illustrated in detail (Figure 23).

As noted in MPEP § 2173.02, the examiner should allow claims which define the patentable subject matter with a "reasonable" degree of particularity and distinctness. Some latitude in the manner of expression and the aptness of terms should be permitted, even though the claim language is not as precise as the examiner might desire. Definiteness of claim language must be analyzed, not in a vacuum, but in light of the content of the disclosure, the teachings of the prior art, and the claim interpretation that would be given by one possessing the ordinary level of skill in the pertinent art at the time the invention was made. While the Office Action suggests that the Examiner may not have completely

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understood the claim language, the Office Action fails to take into consideration the ordinary level of skill of an electrical engineer who is familiar with power on reset circuits and clock circuits. Appellants would respectfully submit that one skilled in the art would understand the claim language without even referring to the supporting specification, as the claims clearly describe the gist of the invention, namely, that operation of clocks are inhibited until voltage stability of the power supply is achieved. When this claim language is further read in light of the details set forth in Appellants' specification, the practice of the invention is abundantly clear to one skilled in the art.

C. The § 102(b) Rejections

The Shaik reference cannot anticipate the present invention, because that reference fails to teach activation of a PLL while inhibiting clock circuits, and then subsequently releasing the hold on the clock circuits once voltage stability has been achieved. Shaik is directed to a clock system for use by a processing unit which has a "sleep" mode in order to save power. Shaik is primarily concerned with power consumption, and with the amount of time that it takes for the circuit to become operative after receiving a "wake-up" signal (i.e., the wake-up time). In the low power mode, the PLL of Shaik is disabled. The oscillator that supplies the primary signal to the PLL may also be disabled, but when the oscillator is additionally disabled, it typically adds to the wake-up time. In order to reduce this wake-up time, Shaik provides two oscillator circuits and control circuitry coupling the different oscillator circuits to the clock output to provide a system clock signal that has a very quick wake-up time. Shaik is not concerned with voltage stability issues as they affect clock circuits. It is furthermore clear that the device of Shaik is not a power on reset circuit.

The Office Action rejects claims 1, 6, 7, and 12 in a conclusory manner, without any corresponding analysis. The Office Action merely states that Shaik shows a "first circuit"

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(referring to the "ENABLE PLL" signal), a starting circuit (referring to element 16 of Shaik), a PLL, and an "inhibitor" (referring to element 10 of Shaik). In setting forth this rejection, the Office Action completely ignores the explicit recitation in the claims regarding the manner in which these components are interconnected, and their functionalities.

For example, the Examiner equates the ENABLE PLL signal of Shaik to the first circuit of Appellants' claim 1. However, claim 1 specifies that this first circuit supplies the voltage for the power on reset circuit. It is clear that the ENABLE PLL signal of Shaik does not provide voltage for any power on reset circuit; indeed, the ENABLE PLL signal of Shaik does not provide power for any component in Shaik. To the contrary, it is used only as an on/off signal which turns on the PLL and the associated oscillator. The first circuit of Appellants' claim 1 does not start the PLL; rather, that is the function of the "starting circuit." Accordingly, the Examiner's attempt to analogize the ENABLE PLL signal of Shaik to Appellants' first circuit is inconsistent with the explicit language of Appellants' claim 1.

Likewise, the Examiner's attempt to equate element 16 of Shaik (the oscillator) with Appellants' "starting circuit" is nonsensical. By the Examiner's own arguments, it is not the oscillator 16 which starts the PLL, but the ENABLE PLL signal line. Additionally, there is no discussion in the Office Action of how the oscillator 16 of Shaik would ostensibly inhibit operation of clock circuits, as required by the language of claim 1. There is also no preset voltage threshold discussed in Shaik. A binary signal (which is provided by the ENABLE PLL signal) does not constitute a "threshold" value. Such a strained interpretation ignores the common and accepted meaning of this term, as well as the meaning of the term as used in Appellants' specification.

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Finally, the Examiner's assertion that element 10 of Shaik is an "inhibitor" is totally unfounded. Element 10 of Shaik is control circuitry that is used to select one of two clock

signals. Shaik never describes that element as an "inhibitor" and never indicates any functionality pertaining to the inhibition of clock circuits. As described at column 3, lines 49-61 of Shaik, control circuitry 10 is simply a multiplexer. This multiplexer selects either the "RINGO" clock signal or the "PLL" clock signal. Clock circuitry 10 does not inhibit anything, and neither does it release anything. In this regard, Appellants' would note that the Examiner is ignoring nearly all of the explicit recitations in claim 1 regarding the purpose and functionality of the claimed elements. A proper construction of the elements of Appellants' independent claims is incompossible with the disclosure of Shaik. Accordingly, the Examiner has not even made out a *prima facie* case of anticipation.

CONCLUSION

Appellants have pointed out with specificity the manifest error in the Examiner's rejections and the claim language which renders the invention patentable over the prior art of record. With respect to both the § 112 first and second paragraph rejections, the Examiner has completely failed to undertake any analysis as to how the claims would be construed by one skilled in the art. Indeed, the Examiner seems to be of the opinion that one skilled in the art is ignorant of common conventional circuits such as power on circuits, phase-locked loops, and threshold detection circuits. Such a perspective is clearly unjustified. With respect to the § 102(b) rejections, the Examiner's analysis fails to take into consideration explicit claim language. A thorough review of the Shaik reference will reveal that it has nothing to do with Appellants' invention, that is, the inhibition of clock circuits until voltage stability has been achieved. In light of the foregoing, it is clear that the Examiner has not made out a *prima facie* case for any of the rejections. It is therefore respectfully requested that this case be

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remanded to the Examiner with instructions to issue a notice of allowance with respect to all pending claims.

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Jack V. Musgrove — Attorney for Applicant(s)

2/28/01 — Date of Signature

Respectfully submitted,

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APPENDIX A

1. (Amended) A power on reset circuit, comprising:

a. a first circuit for applying a first voltage within said power on reset circuit, and

b. a circuit for starting a phase locked loop when voltage applied by said first circuit exceeds a threshold and for inhibiting operation of at least a plurality of clocks until released, and for releasing all inhibited clocks once voltage stability is achieved.

2. The power on reset circuit of claim 1 further comprising a switched converter in which the duty cycle of said switched converter is unity until the output of said switched converter reaches substantially said first voltage.

3. The power on reset circuit of claim 2 in which the duty cycle of said switched converter is programmable.

4. The power on reset circuit of claim 3 in which the duty cycle of said switched converter is reduced from unity after the output of said switched converter reaches substantially said first voltage.

5. The power on reset circuit of claim 3 in which said switched converter settles to a set output voltage before said inhibited clocks are released.

6. The power on reset circuit of claim 1 further comprising a regulator and in which the inhibited clocks are released only after said regulator substantially reaches its stabilized output voltage.

7. (Amended) The power on reset circuit of claim 1, wherein said power on reset circuit is contained within an integrated circuit.

8. A method of applying power to an integrated circuit, comprising the steps of:

a. applying a first voltage to said integrated circuit;

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b. when voltage applied to said integrated circuit exceeds a first threshold, setting the duty cycle of a switched converter to substantially unity and placing a hold on the operation of at least one clock on said integrated circuit;

c. allowing a phase locked loop to start; and

d. when the output of the switched converter nears said first voltage, reducing the duty cycle of said switched converter; and

e. after the output of the switched converter reaches stability, releasing said hold.

9. The method of claim 8 in which the hold on more than one clock is released in stages.

10. The method of claim 8 in which said switched converter is programmable over a bus.

11. The method of claim 10 in which said switched converter is programmable over a communications link exterior to said integrated circuit.

12. A method of applying power to an integrated circuit, comprising the steps of:

a. applying a first voltage to said integrated circuit;

b. when voltage applied to said integrated circuit exceeds a first threshold placing a hold on the operation of at least one clock on said integrated circuit and allowing a phase locked loop to start; and

c. when the output of a regulator reaches stability, releasing said hold.

13. The method of claim 11 in which the hold on more than one clock is released in stages.

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AF/2816

Docket No.: M-11434 US

February 28, 2001

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Re: Applicant(s): Chow, Chung-kai; De Angel, Edwin; Lee, Wai Laing; Page, Joel; Wang, Lei; Zheng, Hong
Assignee: Cirrus Logic, Inc.
Title: Power On Reset Techniques For An Integrated Circuit Chip
Serial No.: ~~09/153~~,364 09-153-864
Examiner: J. Zweizig
Filed: September 16, 1998
Docket No.: **M-11434 US**
Group Art Unit: 2816

Dear Sir:

Transmitted herewith are the following documents in the above-identified application:

(1) Return Receipt Postcard;
(2) This Transmittal Letter (in duplicate); and
(3) Appeal Brief including Appendix A (in triplicate) (15 pgs.).

☒ The fee has been calculated as shown below:

☒	Fee for Appeal Brief	$	310.00
	Total additional fee for this Amendment:	$	310.00

☒ Conditional Petition for Extension of Time: If an extension of time is required for timely filing of the enclosed document(s) after all papers filed with this transmittal have been considered, an extension of time is hereby requested.

☒ Please charge our Deposit Account No. 19-2386 in the amount of $ 310.00

☒ Also, charge any additional fees required and credit any overpayment to our Deposit Account No. 19-2386.

Total: $ 310.00

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner For Patents, Washington, D.C. 20231, on February 28, 2001.

Jack V. Musgrove — Attorney for Applicant(s)
2/28/01 — Date of Signature

Respectfully submitted,

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